Chapter 10 Instructor Notes

Chapter 10 introduces bipolar junction transistors. The material on transistors has been reorganized in this 4th Edition, and is now divided into two independent chapters, one on bipolar devices, and one on field-effect devices. The two chapters are functionally independent, except for the fact that Section 10.1, introducing the concept of transistors as amplifiers and switches, can be covered prior to starting Chapter 11 if the instructor decides to only teach field-effect devices.

Section 10.2 introduces the fundamental ideas behind the operation of bipolar transistors, and illustrates the calculation of the state and operating point of basic transistor circuits. The discussion of the properties of the BJT in Section 10.2 is centered around a description of the base and collector characteristics, and purposely avoids a detailed description of the physics of the device, with the intent of providing an intuitive understanding of the transistor as an amplifier and electronic switch. Example 10.5 introduces the use of Electronics Workbench (EWB) as a tool for analyzing electronics circuits; the CD-ROM contains an introduction to the software package and a number of solved problems.

Section 10.3 introduces large-signal models of the BJT, and also includes the box *Focus on Methodology: Using device data sheets* (pp. 535-537). Example 10.7 (LED Driver) and the box *Focus on Measurements: Large Signal Amplifier for Diode Thermometer* (pp. 539-541) provide two application examples that include EWB solutions.

Section 8.4 introduces the analysis of BJT switches and presents TTL gates.

The end-of-chapter problems are straightforward applications of the concepts illustrated in the chapter.

Learning Objectives

1. Understand the basic principles of amplification and switching. Section 1.
2. Understand the physical operation of bipolar transistors; determine and select the operating point of a bipolar transistor circuit; understand the principle of small signal amplifiers. Section 2.
3. Understand the large-signal model of the bipolar transistor, and apply it to simple amplifier circuits. Section 3.
4. Understand the operation of bipolar transistor as a switch and analyze basic analog and digital gate circuits. Section 4.

Section 10.2: Operation of the Bipolar Junction Transistor

Problem 10.1

Solution:

Known quantities:
Transistor diagrams, as shown in Figure P10.1:

(a) *pnp*, $V_{EB} = 0.6$ V and $V_{EC} = 4.0$ V
(b) *npn*, $V_{CB} = 0.7$ V and $V_{CE} = 0.2$ V
(c) *npn*, $V_{BE} = 0.7$ V and $V_{CE} = 0.3$ V
(d) *pnp*, $V_{BC} = 0.6$ V and $V_{EC} = 5.4$ V

Find:
For each transistor shown in Figure P10.1, determine whether the BE and BC junctions are forward or reverse biased, and determine the operating region.

Analysis:

(a) $V_{BE} = -0.6$ V for a *pnp* transistor implies that the BE junction is forward-biased.

$V_{BC} = V_{EC} - V_{EB} = 3.4$ V. The CB junction is reverse-biased. Therefore, the transistor is in the active region.

(b) $V_{BC} = -0.7$ V for a *npn* transistor implies that the CB junction is reverse-biased.

$V_{BE} = V_{BC} - V_{EC} = -0.5$ V. The BE junction is reverse-biased. Therefore, the transistor is in the cutoff region.

(c) $V_{BE} = 0.7$ V for a *npn* transistor implies that the BE junction is forward-biased.

$V_{BC} = V_{EC} - V_{EB} = 0.4$ V. The CB junction is forward-biased. Therefore, the transistor is in the saturation region.

(d) $V_{BC} = 0.6$ V for a *pnp* transistor implies that the CB junction is reverse-biased.

$V_{BE} = V_{BC} - V_{EC} = -4.8$ V. The BE junction is forward-biased. Therefore, the transistor is in the active region.

Problem 10.2

Solution:

Known quantities:
Transistor type and operating characteristics:

a) *npn*, $V_{BE} = 0.8$ V and $V_{CE} = 0.4$ V
b) *npn*, $V_{CB} = 1.4$ V and $V_{CE} = 2.1$ V
c) *pnp*, $V_{CB} = 0.9$ V and $V_{CE} = 0.4$ V
d) *npn*, $V_{BE} = -1.2$ V and $V_{CB} = 0.6$ V

Find:
The region of operation for each transistor.

Analysis:

a) Since $V_{BE} = 0.8$ V, the BE junction is forward-biased. $V_{CB} = V_{CE} + V_{EB} = -0.4$ V. Thus, the CB junction is forward-biased. Therefore, the transistor is in the saturation region.

b) $V_{BE} = V_{BC} + V_{CE} = 0.7$ V. The BE junction is forward-biased.

$V_{CB} = 1.4$ V. The CB junction is reverse-biased. Therefore, the transistor is in the active region.

c) $V_{CB} = 0.9$ V for a *pnp* transistor implies that the CB junction is forward-biased.

$V_{BE} = V_{BC} - V_{CE} = -1.3$ V. The BE junction is forward-biased. Therefore, the transistor is in the saturation region.

d) With $V_{BE} = -1.2$ V, the BE junction is reverse-biased.

$V_{CB} = -0.6$ V. The CB junction is reverse-biased. Therefore, the transistor is in the cutoff region.

Problem 10.3

Solution:

Known quantities:

The circuit of Figure P10.3. $\beta = \dfrac{I_C}{I_B} = 100$.

Find:

The operating point and the state of the transistor.

Analysis:

$V_{BE} = 0.6$ V and the BE junction is forward biased.

$$I_B = \frac{V_{CC} - V_{BE}}{R_1} = \frac{12 - 0.6}{820} = 13.9\,\mu\text{A}$$

$$I_C = \beta \cdot I_B = 1.39\,\text{mA}$$

Writing KVL around the right-hand side of the circuit:

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0 \quad \Rightarrow$$

$$V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) R_E$$

$$= 12 - (1.39)(2.2) - (1.39 + 0.0139)(0.910)$$

$$= 7.664\,\text{V}$$

$$V_{BC} = V_{BE} + V_{CE} = 0.6 + 7.664 = 8.264\,\text{V}$$

$V_{CE} > V_{BE} \Rightarrow$ The transistor is in the active region.

Problem 10.4

Solution:

Known quantities:
The magnitude of a *pnp* transistor's emitter and base current, and the magnitudes of the voltages across the emitter-base and collector-base junctions:
I_E = 6 mA, I_B = 0.1 mA and V_{EB} = 0.65 V, V_{CB} = 7.3 V.

Find:
a) V_{CE}.
b) I_C.
c) The total power dissipated in the transistor, defined as $P = V_{CE} I_C + V_{BE} I_B$.

Analysis:
a) $V_{CE} = V_{CB} - V_{EB} = 7.3 - 0.65 = 6.65$ V.
b) $I_C = I_E - I_B = 6 - 0.1 = 5.9$ mA.
c) The total power dissipated in the transistor can be found to be: $P \approx V_{CE} I_C = 6.65 \times 5.9 \times 10^{-3} = 39$ mW.

Problem 10.5

Solution:

Known quantities:
The circuit of Figure P10.5, assuming the BJT has $V_\gamma = 0.6\,\text{V}$.

Find:
The emitter current and the collector-base voltage.

Analysis:
Applying KVL to the right-hand side of the circuit, $I_E = -\left(\frac{V_{BE} + 15}{30000}\right) = -\frac{(0.6 + 15))}{30000} = -520\mu\text{A}$

Then, on the left-hand side, assuming $\beta >> 1$:

$$-10 + I_C R_C + V_{CB} = 0 \quad \Rightarrow \quad \begin{aligned} V_{CB} &= 10 - I_C \cdot R_C \\ &= 10 - (-520) \cdot (15) \cdot 10^{-3} \\ &= 17.8\,\text{V} \end{aligned}$$

Problem 10.6

Solution:

Known quantities:
The circuit of Figure P10.6, assuming the BJT has $V_{BE} = 0.6\,\text{V}$ and β =150.

Find:
The operating point and the region in which the transistor operates.

Analysis:

Define $R_C = 3.3\text{k}\Omega,\ R_E = 1.2\text{k}\Omega,\ R_1 = 62\text{k}\Omega,\ R_2 = 15\text{k}\Omega, V_{CC} = 18\,\text{V}$

By applying Thevenin's theorem from base and mass, we have

$$R_B = R_1 \,||\, R_2 = 12.078\ \text{k}\Omega$$

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \cong 3.5\ \text{V}$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + R_E(1+\beta)} \cong 15\ \mu\text{A}$$

$$I_C = \beta I_B = 2.25\ \text{mA}$$

$$V_{CE} = V_{CC} - R_C I_C - R_E I_E = 18 - 3300 \cdot 2.25 \cdot 10^{-3} - 1200 \cdot 151 \cdot 15 \cdot 10^{-6} = 7.857\ \text{V}$$

From the value of V_{CE} it is clear that the BJT is in the active region.

Problem 10.7

Solution:

Known quantities:

The circuit of Figure P10.7, assuming the BJT has $V_\gamma = 0.6\,\text{V}$.

Find:

The emitter current and the collector-base voltage.

Analysis:

Applying KVL to the right-hand side of the circuit,

$$-V_{CC} + I_E R_E + V_{EB} = 0$$

$$I_E = \frac{V_{CC} - V_{EB}}{R_E} = \frac{20 - 0.6}{39 \cdot 10^3} = 497.4\mu\text{A}\ .\ \text{Since}\ \beta >> 1,\ I_C \approx I_E = 497.4\mu\text{A}$$

Applying KVL to the left-hand side: $V_{CB} + I_C R_C - V_{DD} = 0$

$$V_{CB} = V_{DD} - I_C R_C = 20 - 497.4 \cdot 20 \cdot 10^{-3} = 10.05\,\text{V}$$

Problem 10.8

Solution:

Known quantities:

The circuit of Figure P10.7, assuming the emitter resistor is changed to $22\ \text{k}\Omega$ and the BJT has $V_\gamma = 0.6\,\text{V}$.

Find:

The operating point of the transistor.

Analysis:

$$I_E = \frac{V_{CC} - V_{EB}}{R_E} = \frac{20 - 0.6}{22 \cdot 10^3} = 881.8\mu\ \text{A},\ I_C \approx I_E = 881.8\mu\text{A}$$

$$V_{CB} = V_{DD} - I_C R_C = 20 - 881.8 \cdot 20 \cdot 10^{-3} = 2.364\,\text{V}$$

Problem 10.9

Solution:

Known quantities:
The collector characteristics for a certain transistor, as shown in Figure P10.9.

Find:

a) The ratio I_C / I_B for $V_{CE} = 10$ V and $I_B = 100$ μA, 200 μA, and 600 μA

b) V_{CE}, assuming the maximum allowable collector power dissipation is 0.5 W for $I_B = 500$ μA.

Analysis:

a) For $I_B = 100$ μA and $V_{CE} = 10$ V, from the characteristics, we have $I_C = 17$ mA. The ratio I_C / I_B is 170.

For $I_B = 200$ μA and $V_{CE} = 10$ V, from the characteristics, we have $I_C = 33$ mA. The ratio I_C / I_B is 165.

For $I_B = 600$ μA and $V_{CE} = 10$ V, from the characteristics, we have $I_C = 86$ mA. The ratio I_C / I_B is 143.

b) For $I_B = 500$ μA, and if we consider an average β from a., we have $I_C = 159 \cdot 500\ 10^{-3} = 79.5$ mA. The power dissipated by the transistor is $P = V_{CE} I_C + V_{BE} I_B \approx V_{CE} I_C$, therefore:

$$V_{CE} \approx \frac{P}{I_C} = \frac{0.5}{79.5 \cdot 10^{-3}} = 6.29\,\text{V}.$$

Problem 10.10

Solution:

Known quantities:
Figure P10.10, assuming both transistors are silicon-based with $\beta = 100$.

Find:

a) I_{C1}, V_{C1}, V_{CE1}.

b) I_{C2}, V_{C2}, V_{CE2}.

Analysis:

a) From KVL: $-30 + I_{B1} R_{B1} + V_{BE1} = 0 \quad \Rightarrow \quad I_{B1} = \dfrac{30 - 0.7}{750 \cdot 10^3} = 39.07\,\mu\text{A}$

$$I_{C1} = \beta \cdot I_{B1} = 3.907\,\text{mA} \quad \Rightarrow$$

$$V_{C1} = 30 - R_{C1} I_{C1} = 30 - 3.907 \cdot 6.2 = 5.779\,\text{V}$$

$$V_{CE1} = V_{C1} = 5.779\,\text{V}.$$

b) Again, from KVL: $-5.779 + V_{BE2} + I_{E2} R_{E2} = 0 \quad \Rightarrow \quad I_{E2} = \dfrac{5.779 - 0.7}{4.7 \cdot 10^3} = 1.081\,\text{mA}$

and $I_{C2} = I_{E2}\left(\dfrac{\beta}{\beta + 1}\right) = 1.081 \cdot \left(\dfrac{100}{101}\right) = 1.07\,\text{mA}$.

Also, $-30+I_{C2}(R_{C2}+R_{E2})+V_{CE2}=0 \quad \Rightarrow \quad V_{CE2}=30-(1.07)\cdot(20+4.7)=3.574\,\text{V}$.

Finally, $I_{C2}=\dfrac{30-V_{C2}}{R_{C2}} \quad \Rightarrow \quad V_{C2}=30-(1.07)\cdot(20)=8.603\,\text{V}$.

Problem 10.11

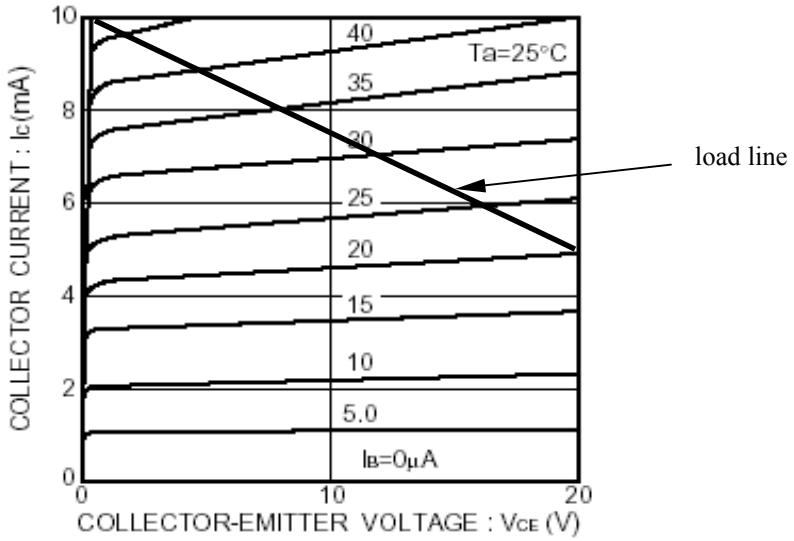
Solution:

Known quantities:
Collector characteristics of the 2N3904 *npn* transistor, see data sheet pg. 536.

Find:
The operating point of the transistor in Figure P10.11, and the value of β at this point.

Analysis:
Construct a load line. Writing KVL, we have: $-50+5000\cdot I_C+V_{CE}=0$.

Then, if $I_C=0$, $V_{CE}=50\,\text{V}$; and if $V_{CE}=0$, $I_C=10\,\text{mA}$. The load line is shown superimposed on the collector characteristic below:

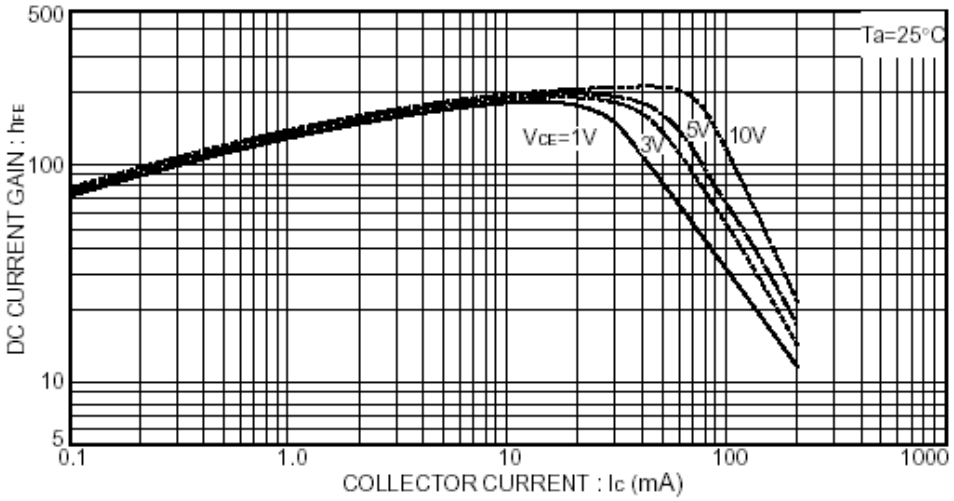


The operating point is at the intersection of the load line and the $I_B=20\mu\text{A}$ line of the characteristic. Therefore, $I_{CQ}\approx 5\,\text{mA}$ and $V_{CEQ}\approx 20\,\text{V}$.

Under these conditions, an $5\,\mu\text{A}$ increase in I_B yields an increase in I_C of approximately $6-5=1\,\text{mA}$. Therefore,

$$\beta\approx\frac{\Delta I_C}{\Delta I_B}=\frac{1\cdot 10^{-3}}{5\cdot 10^{-6}}=200$$

The same result can be obtained by checking the h_{FE} gain from the data-sheets corresponding to 5 mA.



Problem 10.12

Solution:

Known quantities:

The circuit shown in Figure P10.12. With reference to Figure 10.20, assume $V_\gamma = 0.6\,\text{V}$, $V_{sat} = 0.2\,\text{V}$.

Find:

The operating point of the transistor, by computing the ratio of collector current to base current.

Analysis:

$V_{CE} = V_{sat} = 0.2\,\text{V}$, therefore $I_C = \dfrac{10 - 0.2}{R_C} = 9.8\,\text{mA}$

$V_{BE} = V_\gamma = 0.6\,\text{V}$, therefore $I_B = \dfrac{5.7 - 0.6}{R_B} = 102\,\mu\text{A}$

$$\frac{I_C}{I_B} = \frac{9.8 \cdot 10^{-3}}{102 \cdot 10^{-6}} = 96.08 << \beta$$

Problem 10.13

Solution:

Known quantities:

For the circuit shown in Figure P10.13, $V_E = 1\,\text{V}$ and $V_\gamma = 0.6\,\text{V}$.

Find:

a) V_B
b) I_B
c) I_E
d) I_C
e) β
f) α.

Analysis:

a) $V_{EB} = V_E - V_B = V_\gamma = 0.6\,\text{V} \quad \Rightarrow \quad V_B = V_E - V_{EB} = 1 - 0.6 = 0.4\,\text{V}$

b) $I_B = \dfrac{V_B}{R_B} = \dfrac{0.4}{20 \cdot 10^3} = 20\mu\text{A}$

c) $I_E = \dfrac{5 - V_E}{R_E} = \dfrac{5-1}{5000} = 800\mu\text{A}$

d) $I_C = I_E - I_B = 800 - 20 = 780\mu\text{A}$

e) $\beta = \dfrac{I_C}{I_B} = \dfrac{780}{20} = 39$

f) $\alpha = \dfrac{I_C}{I_E} = \dfrac{780}{800} = 0.975$.

Problem 10.14

Solution:

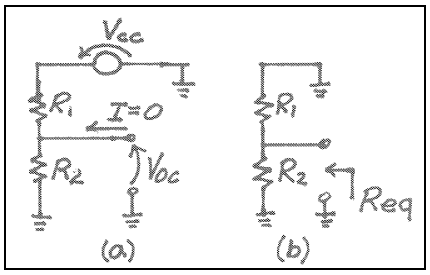
Known quantities:
For the circuit shown in Figure P10.14:

$V_{CC} = 20\,\text{V}$ $\beta = 130$ $R_1 = 1.8\,\text{M}\Omega$ $R_2 = 300\,\text{k}\Omega$ $R_C = 3\,\text{k}\Omega$ $R_E = 1\,\text{k}\Omega$

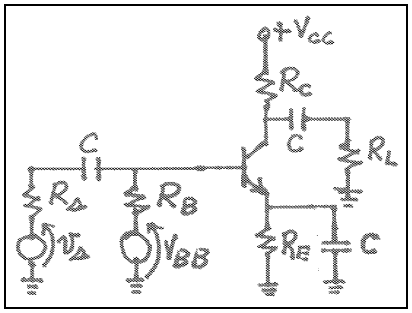
$R_L = 1\,\text{k}\Omega$ $R_S = 0.6\,\text{k}\Omega$ $v_S = \cos\left[6.28\times10^3 \cdot \text{t}\right]\text{mV}$.

Find:
The Thèvenin equivalent of the part of the circuit containing R_1, R_2, and V_{CC} with respect to the terminals of R_2. Redraw the schematic using the Thèvenin equivalent.

Analysis:
Extracting the part of the circuit specified, the Thèvenin equivalent voltage is the open circuit voltage. The equivalent resistance is obtained by suppressing the ideal independent voltage source:



Note that V_{CC} must remain in the circuit because it supplies current to other parts of the circuit:



Problem 10.15

Solution:

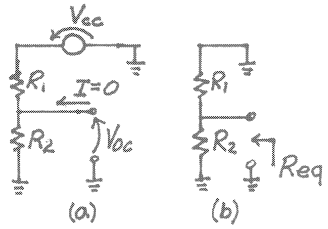
Known quantities:
For the circuit shown in Figure P10.14:

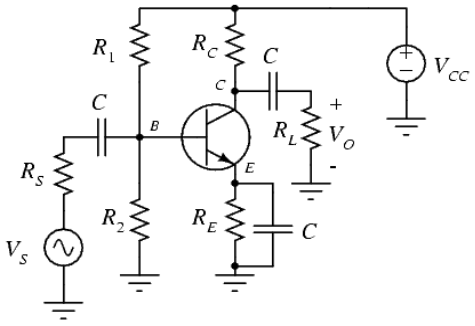
$V_{CC} = 15\,\text{V}$ $\beta = 100$ $R_1 = 68\,\text{k}\Omega$ $R_2 = 11.7\,\text{k}\Omega$ $R_C = 200\Omega$ $R_E = 200\Omega$

$R_L = 1.5\,\text{k}\Omega$ $R_S = 0.9\,\text{k}\Omega$ $v_S = \cos\left[6.28\times10^3 \cdot \text{t}\right]\text{mV}$.

Find:
V_{CEQ} and the region of operation.

Analysis:
Simplify the circuit by obtaining the Thèvenin equivalent of the biasing network in the base circuit:





$$\text{VD}: \; V_{BB} = V_{TH} = \frac{V_{CC}\,R_2}{R_1 + R_2} = \frac{15\cdot 11.7}{68+11.7} = 2.202\,\text{V}$$

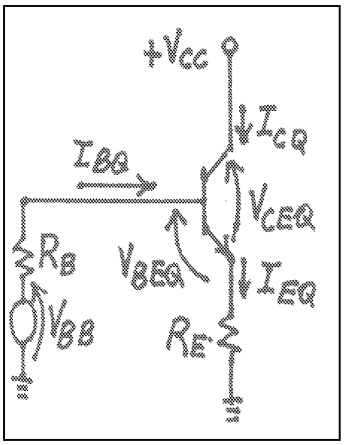
$$\text{Suppress } V_{CC}: \qquad R_B = R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = \frac{68\cdot 11.7}{68+11.7} = 9.982\,\text{k}\Omega$$

Redraw the circuit using the Thèvenin equivalent. The "DC blocking" or "AC coupling" capacitors act as open circuits for DC; therefore, the signal source and load can be neglected since this is a DC problem. Specify directions of current and polarities of voltages. Assume the transistor is operating in its active region; then, the base-emitter junction is forward biased.

$$V_{BEQ} \approx 700\,\text{mV} \quad [Si]$$

$$I_{CQ} = \beta \cdot I_{BQ} \qquad I_{EQ} = (\beta + 1) I_{BQ}$$

Then:



$$\text{KVL: } -V_{BB}+I_{BQ}R_B+V_{BEQ}+I_{EQ}R_E = 0 \;\Rightarrow\; -V_{BB}+I_{BQ}R_B+V_{BEQ}+[\,\beta+1\,]\,I_{BQ}R_E = 0$$

$$I_{BQ} = \frac{V_{BB}-V_{BEQ}}{R_B+[\,\beta+1\,]\,R_E} = \frac{2.202-0.7}{9982+(100+1)(200)} = 49.76\,\mu\text{A}$$

$$I_{CQ} = \beta\, I_{BQ} = 100\cdot 49.76\cdot 10^{-6} = 4.976\,\text{mA}$$

$$I_{EQ} = (\beta+1)\cdot I_{BQ} = (100+1)\cdot 49.76\cdot 10^{-6} = 5.026\,\text{mA}$$

$$\text{KVL: } -I_{EQ}R_E-V_{CEQ}-I_{CQ}R_C+V_{CC} = 0$$

$$V_{CEQ} = V_{CC}-I_{CQ}R_C-I_{EQ}R_E = 15-4.976\cdot 0.2-5.026\cdot 0.2 = 13.00\,\text{V}$$

The collector-emitter voltage is greater than its saturation value (0.3 V for Silicon). Therefore the initial assumption (operation in the active region) was correct and the solution is valid.

Notes:

1. If the collector-emitter voltage were less than its saturation value, the transistor would be operating in its "saturation" or "ohmic" region. In this case, the collector-emitter voltage is equal to its saturation value (0.3 V for Silicon). The solution for the base current remains valid. However, the parameter β and the solution for the collector and emitter curents become invalid. In the saturation region, the base-emitter junction is still forward biased and its voltage remains the same. A solution for the collector and emitter currents is possible using the collector-emitter saturation voltage (0.3 V for Silicon) in a KVL.
2. In the saturation region, the base current has no control over the collector or emitter currents (since β is invalid). Therefore, amplification is impossible.

Problem 10.16

Solution:

Known quantities:

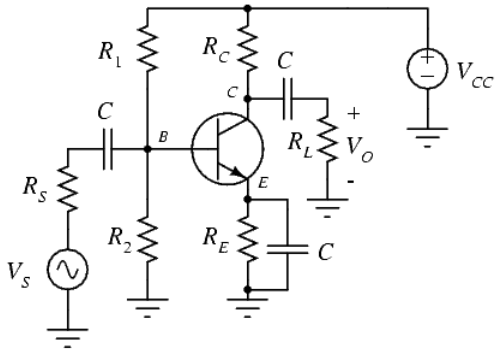
For the circuit shown in Figure P10.14:

$V_{CC}=15\,\text{V}$ $\beta=100$ $R_1=68\,\text{k}\Omega$ $R_2=11.7\,\text{k}\Omega$ $R_C=4\,\text{k}\Omega$ $R_E=200\Omega$

$R_L=1.5\,\text{k}\Omega$ $R_S=0.9\,\text{k}\Omega$ $v_S=\cos\left[6.28\times 10^3\cdot t\right]\text{mV}$.

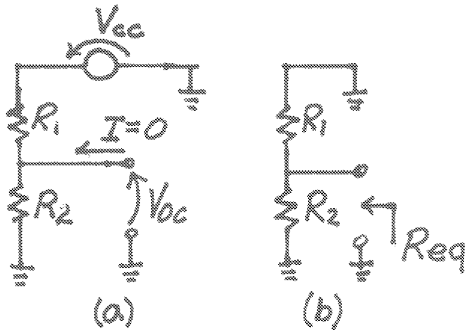
Find:

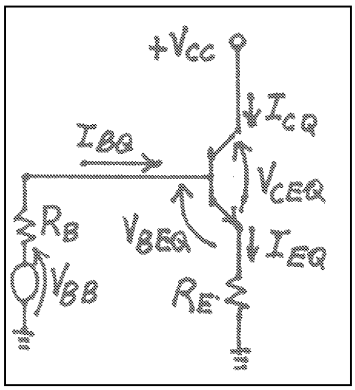
V_{CEQ} and the region of operation.



Analysis:

Simplify the circuit by obtaining the Thèvenin equivalent of the biasing network in the base circuit:





Redraw the circuit using the Thèvenin equivalent. The "DC blocking" or "AC coupling" capacitors act as open circuits for DC; therefore, the signal source and load can be neglected since this is a DC problem. Specify directions of current and polarities of voltages. Assume the transistor is operating in its active region. Then, the base-emitter junction is forward biased.

$$V_{BEQ} \approx 700\,\text{mV} \quad [Si] \qquad I_{CQ} = \beta \cdot I_{BQ} \qquad I_{EQ} = (\beta+1) I_{BQ}$$

$$\text{KVL}: \; -V_{BB} + I_{BQ} R_B + V_{BEQ} + I_{EQ} R_E = 0 \;\Rightarrow\; -V_{BB} + I_{BQ} R_B + V_{BEQ} + [\,\beta+1\,] I_{BQ} R_E = 0$$

$$I_{BQ} = \frac{V_{BB} - V_{BEQ}}{R_B + [\,\beta+1\,] R_E} = \frac{2.202 - 0.7}{9982 + (100+1)(200)} = 49.76\,\mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = 100 \cdot 49.76 \cdot 10^{-6} = 4.976\,\text{mA}$$

$$I_{EQ} = (\beta+1) \cdot I_{BQ} = (100+1) \cdot 49.76 \cdot 10^{-6} = 5.026\,\text{mA}$$

$$\text{KVL}: \; -I_{EQ} R_E - V_{CEQ} - I_{CQ} R_C + V_{CC} = 0$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C - I_{EQ} R_E = 15 - 4.976 \cdot 4 - 5.026 \cdot 0.2 = -5.91\,\text{V}$$

The collector-emitter voltage is less (more negative) than its saturation value (+ 0.3 V for Silicon). Therefore the initial assumption (operation in the active region) was incorrect and the solution is not valid. The device is operating in the saturation region with a saturation collector-emitter voltage equal to 0.3 V. The solutions for the collector and emitter currents are invalid.

THE VALID SOLUTION:

$$\text{KVL}: \; -I_{EQ} R_E - v_{CE\text{-}SAT} - I_{CQ} R_C + V_{CC} = 0 \qquad I_{EQ} = I_{BQ} + I_{CQ}$$

$$-[\,I_{BQ} + I_{CQ}\,] R_E - v_{CE\text{-}SAT} - I_{CQ} R_C + V_{CC} = 0$$

$$I_{CQ} = \frac{V_{CC} - I_{BQ} R_E - v_{CE\text{-}SAT}}{R_E + R_C} = \frac{15 - 49.76 \cdot 0.2 \cdot 10^{-3} - 0.3}{200 + 4000} = 3.498\,\text{mA}$$

The solution for the base current is valid. The value of beta given is not valid.

Problem 10.17

Solution:

Known quantities:
For the circuit shown in Figure P10.17:

$V_{CC} = 12\,\text{V} \quad \beta = 130 \quad R_1 = 82\,\text{k}\Omega \quad R_2 = 22\,\text{k}\Omega \quad R_E = 0.5\,\text{k}\Omega \quad R_L = 16\Omega.$

Find:

V_{CEQ} at the DC operating point.

Analysis:

Simplify the circuit by obtaining the Thèvenin equivalent of the biasing network (R_1, R_2, V_{CC}) in the base circuit:

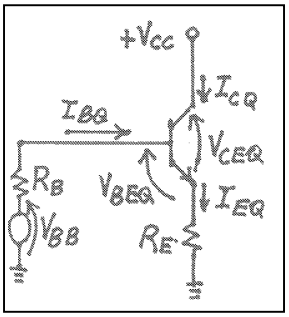
$$\text{VD}: \; V_{BB} = V_{TH} = V_{OC} = \frac{V_{CC}\,R_2}{R_1 + R_2} = \frac{12 \cdot 22}{82 + 22} = 2.538\,\text{V}$$

$$\text{Suppress } V_{CC}: \qquad R_B = R_{eq} = \frac{R_1\,R_2}{R_1 + R_2} = \frac{82 \cdot 22}{82 + 22} = 17.35\,\text{k}\Omega$$

Redraw the circuit using the Thèvenin equivalent. The "DC blocking" or "AC coupling" capacitors act as open circuits for DC; therefore, the signal source and load can be neglected since this is a DC problem. Specify directions of current and polarities of voltages.

Assume the transistor is operating in its active region. Then, the base-emitter junction is forward biased.

$V_{BEQ} \approx 700\,\text{mV} \;\; [Si] \qquad I_{EQ} = [\,\beta + 1\,]\,I_{BQ}$



$$\text{KVL}: \; -V_{BB} + I_{BQ}\,R_B + V_{BEQ} + I_{EQ}\,R_E = 0$$

$$-V_{BB} + I_{BQ}\,R_B + V_{BEQ} + [\,\beta + 1\,]\,I_{BQ}\,R_E = 0$$

$$I_{BQ} = \frac{V_{BB} - V_{BEQ}}{R_B + (\beta + 1) \cdot R_E} = \frac{2.538 - 0.7}{17350 + (130 + 1) \cdot 500} = 22.18\,\mu\text{A}$$

$$I_{EQ} = (\beta + 1)\,I_{BQ} = (130 + 1) \cdot 22.18 \cdot 10^{-6} = 2.906\,\text{mA}$$

$$\text{KVL}: \; -I_{EQ}\,R_E - V_{CEQ} + V_{CC} = 0$$

$$V_{CEQ} = V_{CC} - I_{EQ}\,R_E = 12 - 2.906 \cdot 0.5 = 10.55\,\text{V}$$

The collector-emitter voltage is greater than its saturation value (0.3 V for Silicon). Therefore the initial assumption (operation in the active region) was correct and the solution is valid.

Problem 10.18

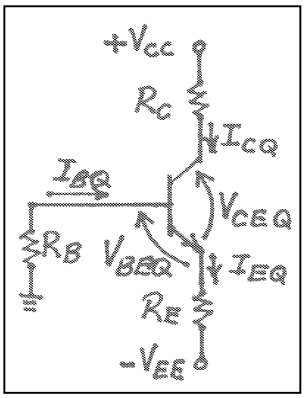
Solution:

Known quantities:
For the circuit shown in Figure P10.18:

$V_{CC} = 12\,\text{V}$ $V_{EE} = 4\,\text{V}$ $\beta = 100$ $R_B = 100\,\text{k}\Omega$ $R_C = 3\,\text{k}\Omega$ $R_E = 3\,\text{k}\Omega$
$R_L = 6\,\text{k}\Omega$ $R_s = 0.6\,\text{k}\Omega$ $v_S = \cos\left[6.28\times10^3 \cdot \text{t}\right]\text{mV}$.

Find:
V_{CEQ} and the region of operation.

Analysis:
The "DC blocking" or "AC coupling" capacitors act as open circuits for DC; therefore, the signal source and load can be neglected since this is a DC problem. Specify directions of current and polarities of voltages. Assume the transistor is operating in its active region; then, the base-emitter junction is forward biased and:



$$V_{BEQ} \approx 700\,\text{mV} \quad [Si]$$

$$I_{CQ} = \beta \cdot I_{BQ} \qquad I_{EQ} = (\beta+1) I_{BQ}$$

$$\text{KVL}: \; -V_{EE} + I_{BQ} R_B + V_{BEQ} + I_{EQ} R_E = 0 \;\Rightarrow$$

$$\Rightarrow \; I_{BQ} = \frac{V_{EE} - V_{BEQ}}{R_B + [\,\beta+1\,] R_E} = \frac{4 - 0.7}{100000 + (100+1)(3000)} = 8.189\;\mu\text{A}$$

$$I_{CQ} = \beta \cdot I_{BQ} = (100)\cdot 8.189\cdot 10^{-6} = 818.9\;\text{mA}$$

$$I_{EQ} = (\beta+1)\cdot I_{BQ} = (100+1)\cdot 8.189\cdot 10^{-6} = 827.0\;\text{mA}$$

$$\text{KVL}: \; +V_{EE} - I_{EQ} R_E - V_{CEQ} - I_{CQ} R_C + V_{CC} = 0$$

$$V_{CEQ} = V_{EE} + V_{CC} - I_{CQ} R_C - I_{EQ} R_E = 4 + 12 - 818.9\cdot 3\cdot 10^{-3} - 827.0\cdot 3\cdot 10^{-3} = 11.06\,\text{V}$$

The collector-emitter voltage is greater (more positive) than its saturation value (+ 0.3 V for Silicon). Therefore the initial assumption (operation in the active region) was correct and the solution is valid.
Notes:
1. DC power may be supplied to an *npn* BJT circuit by connecting the positive terminal of a DC source to the collector circuit, or, by connecting the negative terminal of a DC source to the emitter circuit, or, as was done here, both.
2. In a *pnp* BJT circuit the polarities of the sources must be reversed. Negative to collector and positive to emitter.

Problem 10.19

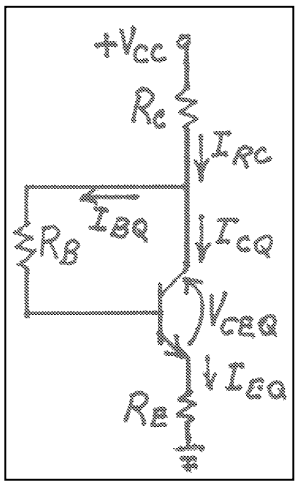
Solution:

Known quantities:
For the circuit shown in Figure P10.19:
$V_{CC} = 12\,\text{V}$ $\beta = 130$ $R_B = 325\,\text{k}\Omega$ $R_C = 1.9\,\text{k}\Omega$ $R_E = 2.3\,\text{k}\Omega$

$R_L = 10\,\text{k}\Omega \qquad R_s = 0.5\,\text{k}\Omega \qquad v_S = \cos\left[6.28\times10^3 \cdot \text{t}\right]\text{mV}$.

Find:

V_{CEQ} and the region of operation.



Analysis:

The "DC blocking" or "AC coupling" capacitors act as open circuits for DC; therefore, the signal source and load can be neglected since this is a DC problem. Specify directions of current and polarities of voltages. Assume the transistor is operating in its active region; then, the base-emitter junction is forward biased. The base and collector currents both flow through the collector resistor in this circuit.

$$V_{BEQ} \approx 700\,\text{mV} \quad [Si]$$

$$I_{CQ} = \beta I_{BQ} \qquad I_{EQ} = [\,\beta+1\,]\, I_{BQ}$$

$$\text{KCL}: \quad I_{BQ} + I_{CQ} - I_{RC} = 0$$

$$I_{RC} = I_{CQ} + I_{BQ} = \beta I_{BQ} + I_{BQ} = [\,\beta+1\,]\, I_{BQ}$$

$$\text{KVL}: \quad -I_{EQ} R_E - V_{BEQ} - I_{BQ} R_B - I_{RC} R_C + V_{CC} = 0$$

$$-[\,\beta+1\,]\, I_{BQ}[\,R_E + R_C\,] - V_{BEQ} - I_{BQ} R_B + V_{CC} = 0$$

$$I_{BQ} = \frac{V_{CC} - V_{BEQ}}{R_B + [\,\beta+1\,][\,R_E + R_C\,]} = \frac{12 - 0.7}{[325 + (130+1)\cdot(2.3+1.9)\,]\cdot10^3} = 12.91\,\mu\text{A}$$

$$I_{RC} = I_{EQ} = [\,\beta+1\,]\, I_{BQ} = (130+1)\cdot12.91\cdot10^{-6} = 1.691\,\text{mA}$$

$$\text{KVL}: \quad -I_{EQ} R_E - V_{CEQ} - I_{RC} R_C + V_{CC} = 0 \quad \Rightarrow$$

$$\Rightarrow \quad V_{CEQ} = V_{CC} - I_{RC} R_C - I_{EQ} R_E = 12 - 1.691\cdot1.9 - 1.691\cdot2.3 = 4.896\,\text{V}$$

The collector-emitter voltage is greater than its saturation value (0.3 V for Silicon). Therefore the initial assumption (operation in the active region) was correct and the solution is valid.

Problem 10.20

Solution:

Known quantities:

For the circuit shown in Figure P10.19:

$V_{CC} = 15\,\text{V} \qquad \text{C} = 0.5\,\mu\text{F} \qquad \beta = 170 \qquad R_B = 22\,\text{k}\Omega \qquad R_C = 3.3\,\text{k}\Omega \qquad R_E = 3.3\,\text{k}\Omega$

$R_L = 1.7\,\text{k}\Omega \qquad R_s = 70\,\Omega \qquad v_S = \cos\left[6.28\times10^3 \cdot \text{t}\right]\text{mV}$.

Find:

V_{CEQ} and the region of operation.

Analysis:

When β is very high (say, greater than 50) the "high beta approximation" can be used, i.e.:

$I_C \approx I_E \approx \beta I_B$

Using this approximation in this problem:

$I_{BQ} \approx 12.5\mu\text{A} \quad I_{CQ} \approx I_{EQ} \approx 2.125\,\text{mA} \quad V_{CEQ} \approx 0.975\,\text{V}$

The collector-emitter voltage is greater than the saturation value (but not by much) so the original assumption (operation in the active region) and the solution are valid. However, when a signal is introduced into the circuit, the collector-emitter voltage will vary about its Q point value. Since the Q point is close to saturation, saturation and severe distortion due to clipping is likely.

Problem 10.21

Solution:

Known quantities:

- For the circuit shown in Figure P10.14:

  $V_{CC} = 15\,\text{V} \quad \text{C} = 0.47\mu\,\text{F} \quad R_1 = 220\,\text{k}\Omega \quad R_2 = 55\,\text{k}\Omega \quad R_C = 3\,\text{k}\Omega$

  $R_E = 710\Omega$

  $R_L = 3\,\text{k}\Omega \quad R_s = 0.6\,\text{k}\Omega \quad v_S = V_{i0} \cdot \sin(\omega t) \quad V_{i0} = 10\,\text{mV}.$

- DC operating point:

  $I_{BQ} = 19.9\mu\,\text{A} \quad V_{CEQ} = 7.61\,\text{V}$

- Transfer characteristic and β of the *npn* silicon transistor:

  $I_C \approx I_s e^{\frac{v_{BE}}{V_T}} = I_s e^{\frac{V_{BEQ} + v_{be}}{V_T}} \qquad \beta = 100$

- Device i-v characteristic plotted in Figure P9.21.

Find:

a) The no-load large signal gain [v_0/v_i].
b) Sketch the waveform of the output voltage as a function of time.
c) How the output voltage is distorted compared with the input waveform.

Analysis:

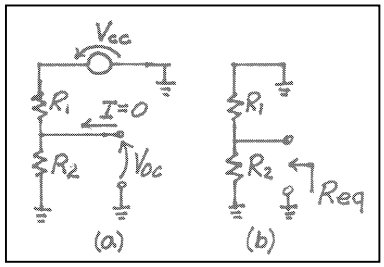
a) Simplify the circuit by determining the Thèvenin equivalent of the biasing network in the base circuit.

$$\text{VD}: \; V_{BB} = V_{TH} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{15 \cdot 55}{220 + 55} = 3.00\,\text{V}$$

Suppress V_{CC}:

$$R_B = R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = \frac{220 \cdot 55 \cdot 10^3}{220 + 55} = 44.0\,\text{k}\Omega$$

First, determine the collector and emitter Q point:



$$\text{KVL}: \quad -I_{EQ}R_E - V_{CEQ} - I_{CQ}R_C + V_{CC} = 0$$

$$V_{CEQ} = -2.010 \cdot 0.710 - 1.990 \cdot 3 + 15 = 7.603\,\text{V}$$

$$I_{CQ} = \beta I_{BQ} = 100 \cdot 19.9 \cdot 10^{-6} = 1.99\,\text{mA}$$

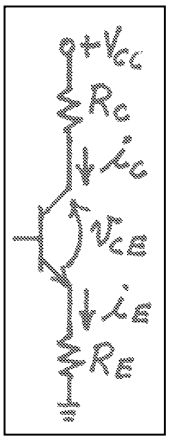
$$I_{EQ} = [\,\beta + 1\,]\, I_{BQ} = 101 \cdot 19.9 \cdot 10^{-6} = 2.01\,\text{mA}$$

Now, determine the DC load line (circuit characteristic).

$$\text{KVL}: \quad -i_E R_E - v_{CE} - i_C R_C + V_{CC} = 0 \qquad i_E = \frac{\beta+1}{\beta} i_C$$

$$i_C = \frac{V_{CC} - v_{CE}}{\frac{\beta+1}{\beta} R_E + R_C} = \frac{V_{CC} - v_{CE}}{3717}$$

$$= \begin{cases} = 0 & \textit{If: } v_{CE} = V_{CC} = 15\,\text{V} \quad \textit{[Intercept 1]} \\ = \dfrac{15}{3717} = 4.035\,\text{mA} & \textit{If: } v_{CE} = 0 \quad \textit{[Intercept 2]} \end{cases}$$



Plot the DC load line on the same plot as the transistor i-v characteristic. Note that the collector current is a linear function of the collector-emitter voltage. Only two points (the two intercepts shown as Points 1 and 2 on the plot) are required to plot a linear function. The DC load line should pass through the Q point.

The AC load line can now be plotted. It will pass through the Q point as does the DC load line; however, its intercepts cannot be directly determined. Instead, its slope will be determined. The slope and the Q point can then be used to plot the AC load line.

$$Slope_{AC} = -\frac{1}{R_C} = -\frac{1}{3000} = -0.3333\,\frac{\text{mA}}{\text{V}} = -\frac{2\text{mA}}{6\text{V}} = \frac{\Delta i_C}{\Delta v_{CE}}$$

For AC the capacitors act as short circuits. The bypass capacitor in parallel with the emitter resistor shorts out any AC voltage across it. The collector coupling capacitor acts as a short and connects the load resistor to the circuit. However, no-load conditions are specified, i.e., the load current is zero or the load resistor is replaced by an open circuit.

With no signal, the circuit operates at its Q point. When a signal is introduced, the operating point changes along the AC load line as a function of the signal voltage. Unfortunately, the device i-v characteristic is plotted as a function of input (base) current instead of voltage.

But, there is the static characteristic that relates collector current to base-emitter voltage:

$$i_C = I_s e^{\frac{v_{BE}}{V_T}} = I_s e^{\frac{V_{BEQ} + v_{be}}{V_T}} = [\,I_s e^{\frac{V_{BEQ}}{V_T}}\,]\; e^{\frac{v_{be}}{V_T}} = I_{CQ} e^{\frac{v_{be}}{V_T}}$$

$$i_B = \frac{i_C}{\beta} = \frac{I_{CQ}}{\beta}\, e^{\frac{v_{be}}{V_T}} = I_{BQ} e^{\frac{v_{be}}{V_T}}$$

The base-emitter signal voltage is related to the input signal voltage. At sufficiently high frequencies (the "mid"-frequency range) the capacitors can be modeled as short circuits for AC. This means that there is no AC voltage across either the AC coupling (DC blocking) capacitor or the capacitor bypassing the emitter resistor. Using superposition to sum only AC voltages around the loop:

$$\text{KVL}: -v_i + v_c + v_{be} + v_e = 0 \qquad v_c = v_e = 0 \qquad \Rightarrow v_{be} = v_i$$

$$i_B = I_{BQ} e^{\frac{v_{be}}{V_T}} = [\,19.9\mu\text{A}\,]\, e^{\frac{v_i}{26\,\text{mV}}}$$

This transfer function can now be used to give the base current as a function of the input voltage. The intersection of the base current curves with the AC load line give the corresponding values of the collector current and collector-emitter voltage (points 3, Q and 4 on the plot):

ωt [rad]	**v_i [mV]**	**i_B [μA]**	**i_C [mA]**	**v_{CE} [V]**	**v_o [V]**
0,π,2π	0	19.9	1.99	7.61	0
π/2	+10	29.23	2.92	4.55	-3.06
3π/2	-10	13.54	1.35	9.15	+1.54

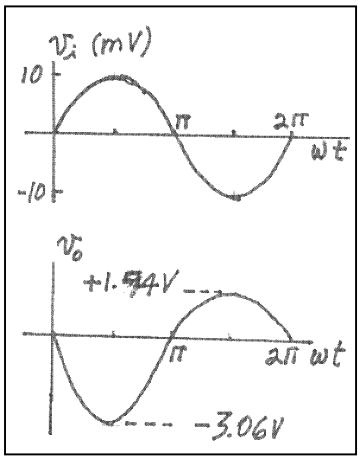
The capacitor connecting the load to the circuit is a DC blocking [and AC coupling] capacitor. Remember that for no load conditions, the load resistor is assumed to be open. Again using superposition to sum only AC voltages around the loop and modeling the capacitors as shorts:

$$-v_e + v_{ce} + v_c + v_o = 0 \qquad v_e = v_c = 0 \quad \Rightarrow \quad v_o = v_{ce} = v_{CE} - V_{CEQ}$$

The no-load voltage gain can be determined using the maximum excursion in the input and output voltages:

$$A_{vo} = \frac{\Delta v_o}{\Delta v_i} = \frac{(-1.54)-(+3.06)}{(10\cdot 10^{-3})-(-10\cdot 10^{-3})} = -230$$

When the input voltage becomes more positive, the output voltage becomes more negative and vice versa. This is called "phase inversion" and is why the gain is negative. In normal amplification this is not important. If the loading effect of the load resistance is included, the AC load line will be steeper and the gain will be reduced.



b) A plot is a large number of calculated points plotted and connected by a smooth curve. In a sketch, only the most significant points [maxima, minima, intercepts, etc] are calculated, plotted, and connected by a carefully drawn smooth curve.

c) The output waveform is very distorted, i.e., it is not a true linearly amplified copy of the input waveform. This is most obvious when the positive and negative peaks of the two curves are compared:

Input voltage	+10 mV	-10 mV
Output voltage	-3.06 V	+1.94 V

The two peaks of the input voltage are equal; however, the positive peak is amplified less than the negative peak. The nonlinear (exponential) behavior of the transistor causes the amplification to be nonlinear and the output waveform to be very distorted. This is characteristic of large signal amplifiers.

Even more serious distortion could occur if the input voltage (also called the "excitation" or "drive") were increased so that saturation or cutoff occurs. This causes "clipping" and a severely distorted output.

Section 10.3: BJT Large-Signal Model

Problem 10.22

Solution:

Known quantities:
For the circuit shown in Figure 10.24:
$V_{off} = 0\,\text{V}, V_{on} = 5\,\text{V}, I_B = 5\,\text{mA}, R_B = 1\,\text{k}\Omega, V_{CC} = 5\,\text{V}, V_\gamma = 0.7\text{V}, V_{CEsat} = 0.2\,\text{V}, \beta = 95,$
$V_{\gamma LED} = 1.4\,\text{V}, I_{LED} \geq 10\,\text{mA}, P_{\max} = 100\,\text{mW}$

Find:
Range of R_C.

Analysis:

$$R_C = \frac{V_{CC} - V_{\gamma LED} - V_{CEsat}}{I_{LED}} \leq \frac{5 - 1.4 - 0.2}{0.01} = 340\ \Omega$$

From the maximum power

$$I_{LED\max} = \frac{P_{\max}}{V_{\gamma LED}} = \frac{0.1}{1.4} = 71\ \text{mA}$$

$$R_C > \frac{V_{CC} - V_{\gamma LED} - V_{CEsat}}{I_{LED\max}} = 47\ \Omega$$

Therefore, $R_C \in [47, 340]\ \Omega$

Problem 10.23

Solution:

Known quantities:
For the circuit shown in Figure 10.26:
$V_D = 1.1\,\text{V}, R_B = 33\,\text{k}\Omega, V_{CC} = 12\,\text{V}, V_{BE} = 0.75\,\text{V}, V_{CEQ} = 6\,\text{V}, \beta = 188.5, R_S = 500\,\Omega$

Find:
The resistance R_C.

Analysis:
The current through the resistance R_B is given by

$$I_B = \frac{V_D - V_{BEQ}}{R_B} = \frac{1.1 - 0.75}{33000} = 10.6\,\mu\text{A}$$

The current through R_S is

$$I_S = \frac{V_{CEQ} - V_D}{R_S} = \frac{6 - 1.1}{500} = 9.8\,\text{mA}$$

It follows that the current through the resistance R_C is

$$I_{CQ} = \beta I_B + I_S = 11.8\,\text{mA}$$

Finally,

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{12 - 6}{0.0118} = 508.5\,\Omega$$

Problem 10.24

Solution:

Known quantities:
For the circuit shown in Figure 10.24:
$V_{off} = 0\,\text{V}, V_{on} = 5\,\text{V}, I_{B\max} = 5\,\text{mA}, R_C = 340\,\Omega, V_{CC} = 5\,\text{V}, V_\gamma = 0.7\text{V}, V_{CEsat} = 0.2\,\text{V}, \beta = 95,$
$V_{\gamma LED} = 1.4\,\text{V}, I_{LED} \geq 10\,\text{mA}, P_{\max} = 100\,\text{mW}$

Find:
Range of R_B.

Analysis:
If the BJT is in saturation

$$I_C = \frac{V_{CC} - V_{\gamma LED} - V_{CEsat}}{R_C} = 10\,\text{mA}$$

In order to guarantee that the BJT is in saturation

$$R_B \leq \frac{V_{on} - V_\gamma}{I_C / \beta} = \frac{5 - 0.7}{\frac{0.01}{95}} = 40.85\,\text{k}\Omega$$

$$R_B \geq \frac{V_{on} - V_\gamma}{I_{B\max}} = 860\,\Omega$$

Problem 10.25

Solution:

Known quantities:
For the circuit shown in Figure 10.24:
$V_{off} = 0\,\text{V}, V_{on} = 5\,\text{V}, I_{B\max} = 5\,\text{mA}, R_B = 10\,\text{k}\Omega, R_C = 340\Omega, V_{CC} = 5\,\text{V}, V_\gamma = 0.7\text{V}, V_{CEsat} = 0.2\,\text{V},$
$V_{\gamma LED} = 1.4\,\text{V}, I_{LED} \geq 10\,\text{mA}, P_{\max} = 100\,\text{mW}$

Find:
Minimum value of β that will ensure the correct operation of the LED.

Analysis:

$$I_B = \frac{V_{on} - V_\gamma}{R_B} = \frac{4.3}{10000} = 0.43\,\text{mA}$$

$$\beta_{\min} = \frac{I_{LED\min}}{I_B} = \frac{0.01}{0.43 \cdot 10^{-3}} = 23.25$$

Problem 10.26

Solution:

Known quantities:
For the circuit shown in Figure 10.24:
$V_{off} = 0\,\text{V}, V_{on} = 3.3\,\text{V}, I_{B\max} = 5\,\text{mA}, R_B = 10\,\text{k}\Omega, R_C = 340\Omega, V_{CC} = 5\,\text{V}, V_\gamma = 0.7\text{V}, V_{CEsat} = 0.2\,\text{V},$
$V_{\gamma LED} = 1.4\,\text{V}, I_{LED} \geq 10\,\text{mA}, P_{\max} = 100\,\text{mW}$

Find:
Minimum value of β that will ensure the correct operation of the LED.

Analysis:

$$I_B = \frac{V_{on} - V_\gamma}{R_B} = \frac{3.3 - 0.7}{10000} = 0.26\,\text{mA}$$

$$\beta_{\min} = \frac{I_{LED\min}}{I_B} = \frac{0.01}{0.26 \cdot 10^{-3}} = 38.5$$

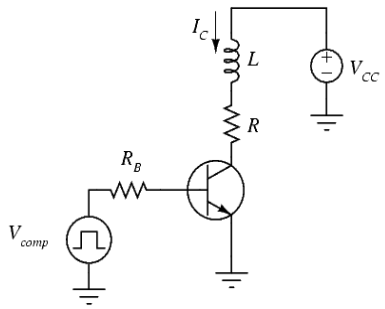
Problem 10.27

Solution:

Known quantities:
For the circuit shown in Figure 10.24:
$V_{off} = 0\,\text{V}, V_{on} = 5\,\text{V}, I_{B\max} = 1\,\text{mA}, R_B = 1\,\text{k}\Omega, R = 12\,\Omega, V_{CC} = 13\,\text{V}, V_\gamma = 0.7\text{V}, V_{CEsat} = 1\,\text{V},$
$I_C \geq 1\,\text{A}$

Find:
Minimum value of β that will ensure the correct operation of the fuel injector.

Analysis:



$$I_C = \frac{V_{CC} - V_{CEsat}}{R} = \frac{13 - 1}{12} = 1\,\text{A}$$

$$\beta_{\min} = \frac{I_C}{I_{B\max}} = \frac{1}{1 \cdot 10^{-3}} = 1000$$

Problem 10.28

Solution:

Known quantities:
For the circuit shown in Figure 10.24:
$V_{off} = 0\,\text{V}, V_{on} = 5\,\text{V}, I_{B\max} = 1\,\text{mA}, \beta = 2000, R = 12\,\Omega, V_{CC} = 13\,\text{V}, V_\gamma = 0.7\text{V}, V_{CEsat} = 1\,\text{V},$
$I_C \geq 1\,\text{A}$

Find:
The range of R_B that will ensure the correct operation of the fuel injector.

Analysis:
If the BJT is in saturation

$$I_C = \frac{V_{CC} - V_{CEsat}}{R} = 1\,\text{A}$$

Because this is the minimum value allowed for the current to drive the fuel injector, it is necessary to guarantee that the BJT is in saturation.
In order to guarantee that the BJT is in saturation

$$R_B \le \frac{V_{on} - V_\gamma}{I_C / \beta} = \frac{5 - 0.7}{\frac{1}{2000}} = 8.6\,\text{k}\Omega$$

$$R_B \ge \frac{V_{on} - V_\gamma}{I_{B\max}} = 4.3\,\text{k}\Omega$$

Problem 10.29

Solution:

Known quantities:
For the circuit shown in Figure 10.24:

$V_{off} = 0\,\text{V}, V_{on} = 3.3\,\text{V}, I_{B\max} = 1\,\text{mA}, \beta = 2000, R = 12\,\Omega, V_{CC} = 13\,\text{V}, V_\gamma = 0.7\text{V}, V_{CEsat} = 1\,\text{V},$
$I_C \ge 1\,\text{A}$

Find:
The range of R_B that will ensure the correct operation of the fuel injector.

Analysis:
If the BJT is in saturation

$$I_C = \frac{V_{CC} - V_{CEsat}}{R} = 1\,\text{A}$$

Because this is the minimum value allowed for the current to drive the fuel injector, it is necessary to guarantee that the BJT is in saturation.
In order to guarantee that the BJT is in saturation

$$R_B \le \frac{V_{on} - V_\gamma}{I_C / \beta} = \frac{3.3 - 0.7}{\frac{1}{2000}} = 5.2\,\text{k}\Omega$$

$$R_B \ge \frac{V_{on} - V_\gamma}{I_{B\max}} = 2.6\,\text{k}\Omega$$

Section 10.4: BJT Switches and Gates

Problem 10.30

Solution:

Known quantities:
The circuit given in Figure P10.30.

Find:
Show that the given circuit functions as an OR gate if the output is taken at v_{01}.

Analysis:
Construct a state table. This table clearly describes an AND gate when the output is taken at v_{o1}.

v_1	v_2	Q_1	Q_2	Q_3	v_{o1}	v_{o2}
0	0	off	off	on	0	5V
0	5V	off	on	off	5V	0
5V	0	on	off	off	5V	0
5V	5V	on	on	off	5V	0

Problem 10.31

Solution:

Known quantities:
The circuit given in Figure P10.30.

Find:
Show that the given circuit functions as a NOR gate if the output is taken at v_{02}.

Analysis:
See the state table constructed for Problem 10.30. This table clearly describes a NOR gate when the output is taken at v_{o2}.

Problem 10.32

Solution:

Known quantities:
The circuit given in Figure P10.32.

Find:
Show that the given circuit functions as an AND gate if the output is taken at v_{01}.

Analysis:
Construct a state table. This table clearly describes an AND gate when the output is taken at v_{o1}.

v_1	v_2	Q_1	Q_2	Q_3	v_{o1}	v_{o2}
0	0	off	off	on	0	5V
0	5V	off	on	on	0	5V
5V	0	on	off	on	0	5V
5V	5V	on	on	off	5V	0

Problem 10.33

Solution:

Known quantities:
The circuit given in Figure P10.32.

Find:
Show that the given circuit functions as a NAND gate if the output is taken at v_{02}.

Analysis:
See the state table constructed for Problem 10.32. This table clearly describes a NAND gate when the output is taken at v_{o2}.

Problem 10.34

Solution:

Known quantities:
In the circuit given in Figure P10.34 the minimum value of v_{in} for a high input is 2.0 V. Assume that the transistor Q_1 has a β of at least 10.

Find:
The range for resistor R_B that can guarantee that the transistor is on.

Analysis:

$i_c = \dfrac{5-0.2}{2000} = 2.4\,\text{mA}$, therefore, $i_B = i_C/\beta = 0.24$ mA.

$(v_{in})\text{min} = 2.0$ V and $(v_{in})\text{max} = 5.0$ V, therefore, applying KVL: $-v_{in} + R_B\, i_B + 0.6 = 0$

or $R_B = \dfrac{v_{in} - 0.6}{i_B}$. Substituting for $(v_{in})\text{min}$ and $(v_{in})\text{max}$, we find the following range for R_B:

$$5.833k\Omega \le R_B \le 18.333k\,\Omega$$

Problem 10.35

Solution:

Known quantities:
For the circuit given in Figure P10.35: $R_{1C} = R_{2C} = 10\,\text{k}\Omega$, $R_{1B} = R_{2B} = 27\,\text{k}\Omega$.

Find:
a) v_B, v_{out}, and the state of the transistor Q_1 when v_{in} is low.
b) v_B, v_{out}, and the state of the transistor Q_1 when v_{in} is high.

Analysis:

a) v_{in} is low $\Rightarrow Q_1$ is cutoff $\Rightarrow v_B = 5$ V $\Rightarrow Q_2$ is in saturation $\Rightarrow v_{out} = low = 0.2$ V.

b) v_{in} is high $\Rightarrow Q_1$ is in saturation $\Rightarrow v_B = 0.2$ V $\Rightarrow Q_2$ is cutoff $\Rightarrow v_{out} = high = 5$ V.

Problem 10.36

Solution:

Known quantities:

For the inverter given in Figure P10.36: $R_{C1} = R_{C2} = 2\,\text{k}\Omega$, $R_B = 5\,\text{k}\Omega$.

Find:

The minimum values of β_1 and β_2 to ensure that Q_1 and Q_2 saturate when v_{in} is high.

Analysis:

$i_c = \dfrac{5-0.2}{2000} = 2.4\,\text{mA}$, therefore, $i_c = \dfrac{2.5}{\beta}\,\text{mA}$. Applying KVL:

$-5 + R_B i_{B1} + 0.6 + 0.6 + 0.6 = 0$

Therefore, $i_{B1} = 0.64$ mA. $i_{E1} = \beta_1 \cdot i_{B1} = {}^{600}\!/_{500} + i_{B2}$ or $0.64 \cdot \beta_1 = 1.2 + {}^{2.5}\!/_{\beta_2}$

Choose $\beta_2 = 10 \Rightarrow \beta_1 = 2.27$.

Problem 10.37

Solution:

Known quantities:

For the inverter given in Figure P10.36: $R_{C1} = 2.5\,\text{k}\Omega$, $R_{C2} = 2\,\text{k}\Omega$, $\beta_1 = \beta_2 = 4$.

Find:

Show that Q_1 saturates when v_{in} is high. Find a condition for R_{C2} to ensure that Q_2 also saturates.

Analysis:

$i_{B1} = \dfrac{3.2}{4000} = 0.8\,\text{mA} \Rightarrow i_{C1} = 3.2\,\text{mA}$

Applying KCL: $\dfrac{600}{500} + i_{B2} = 3.2 \Rightarrow i_{B2} = 2\,\text{mA}$; $i_{C2} = \beta \cdot i_{B2} = 8\,\text{mA}$

Applying KVL: $5 - 0.2 = 0.008 \cdot R_{C2} \Rightarrow R_{C2} = 600\Omega$

Problem 10.38

Solution:

Known quantities:

The basic circuit of a TTL gate, shown in Figure P10.38.

Find:

The logic function performed by this circuit.

Analysis:

The circuit performs the function of a 2-input NAND gate. The analysis is similar to Example 10.8.

Problem 10.39

Solution:

Known quantities:
The circuit diagram of a three-input TTL NAND gate, given in Figure P10.39.

Find:

v_{B1}, v_{B2}, v_{B3}, v_{C2}, and v_{out}, assuming that all the input voltages are high.

Analysis:

Q_2 and Q_3 conduct, while Q_4 is cutoff. $v_{B1} = 1.8$ V, $v_{B2} = 1.2$ V, $v_{B3} = 0.6$ V, and $v_{C2} = v_{out} = 0.2$ V.

Problem 10.40

Solution:

Known quantities:
Figure P10.40.

Find:
Show that when two or more emitter-follower outputs are connected to a common load, as shown in Figure P10.54, the OR operation results; that is, $v_0 = v_1$ OR v_2.

Analysis:

v_2	v_1	Q_1	Q_2	v_0
L	L	L	L	L
L	H	H	L	H
H	L	L	H	H
H	H	H	H	H

L : Low; H : High.
