Chapter 11 Instructor Notes

Chapter 11 introduces field-effect transistors. The material on transistors has been reorganized in this 4th Edition, and is now divided into two independent chapters, one on bipolar devices, and one on field-effect devices. The two chapters are functionally independent, except for the fact that Section 10.1, introducing the concept of transistors as amplifiers and switches, can be covered prior to starting Chapter 11 if the instructor decides to only teach field-effect devices.

Section 11.1 briefly reviews the classification and symbols for the major families of field-effect devices. Section 11.2 introduces the fundamental ideas behind the operation of N-channel field-effect enhancement-mode transistors, and illustrates the calculation of the state and operating point of basic field-effect transistor circuits. A brief explanation of P-channel devices is also presented in this section. Section 11.3 briefly outlines the operation of MOSFET amplifiers. Section 11.4 introduces the analysis of MOSFET switches and presents CMOS gates. The box *Focus on Measurements: MOSFET bidirectional analog gate* (pp. 572-573) presents ananalog application of CMOS technology.

The end-of-chapter problems are straightforward applications of the concepts illustrated in the chapter.

Learning Objectives

1. Understand the classification of field-effect transistors. Section 1.
2. Learn the basic operation of enhancement-mode MOSFETs by understanding their *i-v* curves and defining equations. Section 2.
3. Learn how enhancement-mode MOSFET circuits are biased. Section 2.
4. Understand the concept and operation of FET amplifiers. Section 3
5. Understand the concept and operation of FET switches. Section 4.
6. Analyze FET switches and digital gates. Section 4.

Section 11.2: n-channel MOSFET Operation

Problem 11.1

Solution:

Known quantities:

For the transistors shown in Figure P11.1, $|V_T| = 3\,\text{V}$.

Find:

The operating state of each transistor.

Analysis:

a) This is an n-channel enhancement MOSFET, with $V_T = -3\ \text{V}$. To operate in the triode region, the condition is: $v_{DS} < v_{GS} - V_T$. To operate in the saturation region, the condition is: $v_{DS} \geq v_{GS} - V_T$. To turn the transistor on, the condition is: $v_{GS} > V_T$.

We can compute: $v_{GS} = -2.5\,\text{V}$ $v_{DS} = 2.5\,\text{V}$

$$v_{GS} - V_T = -2.5 + 3 = 0.5\,\text{V}$$

$$v_{DS} = 2.5\,\text{V} > v_{GS} - V_T = 0.5\,\text{V}.$$

Therefore, the transistor is in the saturation region.

b) This is a p-channel enhancement MOSFET, with $V_T = 3\ \text{V}$. To operate in the triode region, the condition is: $v_{DS} > v_{GS} - V_T$. To operate in the saturation region, the condition is: $v_{DS} \leq v_{GS} - V_T$. To turn the transistor on, the condition is: $v_{GS} < V_T$.

We can compute: $v_{GS} = 2\,\text{V}$ $v_{DS} = -1\,\text{V}$

$$v_{GS} - V_T = 2 - 3 = -1\,\text{V}$$

$$v_{DS} = -1\,\text{V} = v_{GS} - V_T = -1\,\text{V}.$$

Therefore, the transistor is in the saturation region.

c) This is a p-channel enhancement MOSFET, with $V_T = -3\ \text{V}$. To operate in the triode region, the condition is: $v_{DS} > v_{GS} - V_T$. To operate in the saturation region, the condition is: $v_{DS} \leq v_{GS} - V_T$. To turn the transistor on, the condition is: $v_{GS} < V_T$.

We can compute: $v_{GS} = -5\,\text{V}$ $v_{DS} = -1\,\text{V}$

$$v_{GS} - V_T = -5 + 3 = -2\,\text{V}$$

$$v_{DS} = -1\,\text{V} > v_{GS} - V_T = -2\,\text{V}.$$

Therefore, the transistor is in the triode region.

d) This is an n-channel enhancement MOSFET, with $V_T = -3\ \text{V}$. To operate in the triode region, the condition is: $v_{DS} < v_{GS} - V_T$. To operate in the saturation region, the condition is: $v_{DS} \geq v_{GS} - V_T$. To turn the transistor on, the condition is: $v_{GS} > V_T$.

We have: $v_{GS} = -2V > V_T$.

$$v_{GS} - V_T = -2 + 3 = 1V$$

$$v_{DS} = 6V > v_{GS} - V_T = 1V$$

Therefore, the transistor is in the saturation region.

Problem 11.2

Solution:

Known quantities:

The potentials of an n-channel enhancement-mode MOSFET (4, 5, and 10 V respectively).

Find:

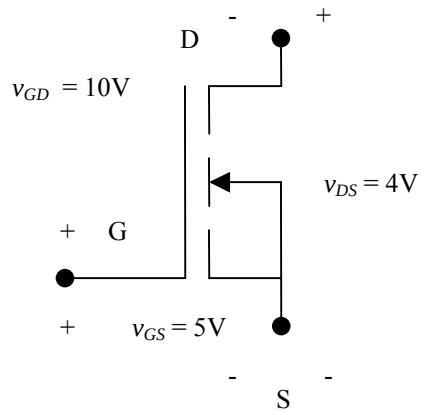
The circuit symbol, if the device is operating:

a) In the ohmic state.
b) In the active region.

Analysis:

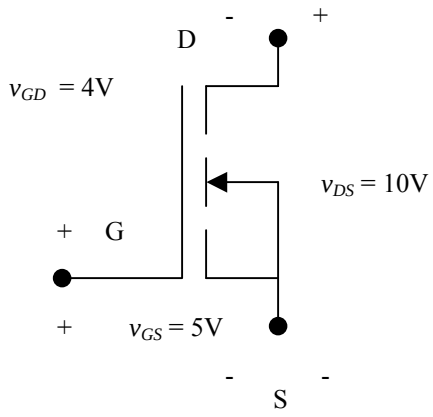
a) To operate in the ohmic region, the condition is: $v_{DS} < v_{GS} - V_T$ and $V_T > 0,\ v_{DS} > 0$.

The circuit for operation in the ohmic region is shown below.



b) To operate in the active region, the condition is: $v_{DS} \geq v_{GS} - V_T$ and $V_T > 0,\ v_{DS} > 0$.

The circuit for operation in the active region is shown below.



Problem 11.3

Solution:

Known quantities:

The threshold voltage, $V_T = 2$ V, of an enhancement-type NMOS that has its source grounded and a 3 V DC source connected to the gate.

Find:
The operating state if:

a) $v_D = 0.5\,\text{V}$.

b) $v_D = 1\,\text{V}$.

c) $v_D = 5\,\text{V}$

Analysis:

$v_{DS} = v_D = 0.5\,\text{V}$

a) $v_{GS} - V_T = 3 - 2 = 1\,\text{V}$

$v_{DS} < v_{GS} - V_T$

The transistor is in the triode region.

$v_{DS} = v_D = 1\,\text{V}$

b) $v_{GS} - V_T = 3 - 2 = 1\,\text{V}$

$v_{DS} = v_{GS} - V_T$

The transistor is either in the triode or in the saturation region.

$v_{DS} = v_D = 5\,\text{V}$

c) $v_{GS} - V_T = 3 - 2 = 1\,\text{V}$

$v_{DS} > v_{GS} - V_T$

The transistor is in the saturation region.

Problem 11.4

Solution:

Known quantities:

The threshold voltage, $V_T = 2$ V, of the p-channel transistor shown in Figure P11.4. $k = 10\,\text{mA/V}^2$.

Find:

R and v_D for $i_d = 0.4\,\text{mA}$.

Analysis:

The device shown is a p-channel enhancement mode MOSFET, with , $V_T = 2$ V and , $V_{DG} = 0$ V. To operate in the saturation region we require: $v_{DS} \geq v_{GS} - V_T$.

Since $v_{DG} = v_{DS} - v_{GS} = 0 > -V_T = -2\,\text{V}$, the transistor is in the saturation region. Knowing $k = 10\,\text{mA/V}^2$, we can write: $0.4 = 10 \cdot (v_{GS} - 2)^2$ and determine $v_D = v_{DS} = v_{GS} = 2.2\,\text{V}$. R can be found as follows:

$$R = \frac{20 - v_D}{i_D} = \frac{20 - 2.2}{0.4 \cdot 10^{-3}} = 44.5\,\text{k}\Omega$$

Problem 11.5

Solution:

Known quantities:

The threshold voltage, $V_T = 2$ V, of an enhancement-type NMOS transistor. $i_D = 1$ mA when $v_{GS} = v_{DS} = 3$ V.

Find:
The value of i_D for $v_{GS} = 4$ V.

Analysis:
Because $v_{DS} > v_{GS} - V_T$, the transistor is in the saturation region:

$$i_D = k \cdot (v_{GS} - V_T)^2 = k \cdot (3-2)^2 = 0.001\text{A}$$
$$\Rightarrow \quad k = 0.001.$$

For $v_{GS} = 4$ V we have:

$$i_D = 0.001 \cdot (4-2)^2 = 4\text{mA}.$$

Problem 11.6

Solution:

Known quantities:
Characteristics of an n-channel enhancement-mode MOSFET operated in the ohmic region:

$v_{DS} = 0.4$ V, $V_T = 3.2$ V. Effective resistance of the channel, given by: $R_{DS} = \dfrac{500}{(v_{GS} - 3.2)}\Omega$.

Find:
The value of i_D when $v_{GS} = 5$ V, $R_{DS} = 500\ \Omega$, and $v_{GD} = 4$ V.

Analysis:
Since $V_{DS} = 0.4 < v_{GS} - V_T = 5 - 3.2 = 1.8\text{V}$ the transistor is operating in the ohmic region. The effective resistance is: $R_{DS} = \dfrac{500}{(5-3.2)} = 277.78\Omega$. Since $R_{DS} = \dfrac{V_{DS}}{i_D}$, we have:

$$i_D = \frac{V_{DS}}{R_{DS}} = 1.44\text{mA}.$$

Problem 11.7

Solution:

Known quantities:
The threshold voltage, $V_T = 2.5$ V, of an enhancement-type NMOS that has its source grounded and a 4 V DC source connected to the gate.

Find:
The operating state if:

a) $v_D = 0.5\text{V}$

b) $v_D = 1.5\text{V}$.

Analysis:

a) $v_{DS} = 0.5 < v_{GS} - V_T = 4 - 2.5 = 1.5$ V, therefore the transistor is in the triode region.

b) $v_D = 1.5$ V $= v_{DS}$, therefore the transistor is at the border of the saturation and triode regions.

Problem 11.8

Solution:

Known quantities:

The threshold voltage, $V_T = 4$ V, of an enhancement-type NMOS. $i_D = 1$ mA when $v_{GS} = v_{DS} = 6$ V.

Find:

The value of i_D when $v_{GS} = 5$ V.

Analysis:

From $0.001 = k(6 - 4)^2$, we have $k = 0.25\times10^{-3}$

For $v_{GS} = 5$ V, and assuming active operation: $i_D = 0.25\times10^{-3}(5 - 4)^2 = 0.25$ mA.

Problem 11.9

Solution:

Known quantities:

The threshold voltage, $V_T = 1.5$ V, of the NMOS transistor shown in Figure P11.9. $k = 0.4\,\text{mA/V}^2$.

Find:

The voltage levels of the pulse signal at the drain output, if v_G is a pulse with 0 V to 5 V.

Analysis:

Since $V_T = 1.5$ V, with $v_G = 0$ V, $v_{GS} < V_T$, the transistor is cut off. Therefore, $v_D = 5$ V.

When $v_G = 5$ V, and assuming that the transistor is in the active region:

$i_D = k\,(v_{GS} - V_T)^2 = 0.4\,(5 - 1.5)^2 = 4.9$ mA. Therefore, $v_D = 5 - 4.9\times1 = 0.1$ V.

Section 11.3: n-channel MOSFET Amplifiers

Problem 11.10

Solution:

Known quantities:
The *i-v* characteristic of Figure P11.10(a), and the circuit in Figure P11.10(b):
$V_{GG} = 7\,\text{V}, V_{DD} = 10\,\text{V}, R_D = 5\,\Omega$

Find:
The current i_{DQ} the voltage v_{DSQ}, and the region of operation of the MOSFET.

Analysis:
The operating point can be determined using the load line method.

$$i_D = \frac{V_{DD}}{R_D} - \frac{v_{DS}}{R_D} = 2 - 0.2\,v_{DS}$$

By superimposing the load line on Figure P11.10(a), and by noticing that $V_{GS} = V_{GG} = 7\,\text{V}$, we obtain

$i_{DQ} = 0.8\,\text{A}, v_{DSQ} = 6\,\text{V}$

The MOSFET is in the saturation region.

Problem 11.11

Solution:

Known quantities:
The circuit in Figure P11.10(b):
$V_{GG} = 7\,\text{V}, V_{DD} = 20\,\text{V}, V_T = 3\,\text{V}, R_D = 5\,\Omega, K = 50\,\text{mA/V}^2$

Find:
The current i_{DQ} the voltage v_{DSQ}, and the region of operation of the MOSFET.

Analysis:
Assuming that the MOSFET is in the saturation region, the quiescent drain current is

$$i_{DQ} = K(v_{GSQ} - V_T)^2 = 0.05(7-3)^2 = 0.8\,\text{A}$$

The drain-to-source voltage is

$$v_{DSQ} = V_{DD} - R_D i_{DQ} = 20 - 5 \cdot 0.8 = 16\,\text{V}$$

Since $v_{DG} = v_{DS} - v_{GS} = 9\text{V} > V_T \Rightarrow$ hypothesis was correct

---

Problem 11.12

Solution:

Known quantities:
The circuit in Figure 11.12:
$V_{DD} = 36\,\text{V}, V_T = 4\,\text{V}, R_D = 10\,\text{k}\Omega, R_1 = R_2 = 2\,\text{M}\Omega, K = 0.1\,\text{mA/V}^2$

Find:
The current i_{DQ}, the voltage v_{DSQ}, the resistance R_S, and the operating region of the MOSFET.

Analysis:
Using Thevenin equivalent,

$$V_{GG} = \frac{R_2}{R_1 + R_2} V_{DD} = 18 \text{ V}$$

We can write the equations

$$V_{GG} = v_{GSQ} + R_S i_{DQ} = 18,$$

$$V_{DD} = (R_D + R_S) i_{DQ} + v_{DSQ} = R_D i_{DQ} + 18 - v_{GSQ} + v_{DSQ} = 36 \Rightarrow R_D i_{DQ} + v_{DSQ} = 18 + v_{GSQ}$$

Assuming saturation conditions, the current i_D can be written as

$$i_{DQ} = K(v_{GSQ} - V_T)^2 \Rightarrow v_{GSQ} + R_S K(v_{GSQ} - V_T)^2 = 18$$

and

$$R_D K(v_{GSQ} - V_T)^2 + v_{DSQ} = 18 + v_{GSQ}$$

Notice that the problem has more unknown than equations; we can impose the v_{DSQ} to ensure saturation conditions as

$$v_{DSQ} = V_{DD} / 2 = 18 \text{ V} \Rightarrow$$

$$(v_{GSQ} - V_T)^2 = v_{GSQ} \Rightarrow v_{GSQ}^2 - 9 v_{GSQ} + 16 = 0 \Rightarrow v_{GSQ} = 6.56 \text{ V}$$

Remark: The other solution of the algebraic equation is not acceptable because < V_T.

The resistance R_S is given by

$$R_S = \frac{18 - v_{GSQ}}{K\left(v_{GSQ} - V_T\right)^2} = \frac{18 - 6.56}{0.1 \cdot 10^{-3}\left(6.56 - 4\right)^2} = 17.45 \text{ k}\Omega$$

and the drain current

$$i_{DQ} = K(v_{GSQ} - V_T)^2 = 0.655 \text{ mA}$$

Problem 11.13

Solution:

Known quantities:
n-channel MOSFET operating in saturation region with

$$v_{DSQ} = 5 \text{ V}, v_{GSQ} = 3 \text{ V}, V_T = 1 \text{ V}, K = 0.1 \text{ mA/V}^2$$

Find:
The transconductance g_m.

Analysis:
The drain current is

$$i_{DQ} = K(v_{GSQ} - V_T)^2 = 0.4 \text{ mA}$$

The transconductance is

$$g_m = 2\sqrt{K i_{DQ}} = 2\sqrt{0.04} \cdot 10^{-3} = 0.4 \text{ mA/V}^2$$

Problem 11.14

Solution:

Known quantities:
The circuit in Figure 11.12:

$$V_{DD} = 12 \text{ V}, V_T = 1 \text{ V}, R_S = R_D = 10 \text{ k}\Omega, R_1 = R_2 = 2 \text{ M}\Omega, K = 1 \text{ mA/V}^2$$

Find:
The current i_{DQ}, the voltage v_{DSQ}, and the voltage v_{GSQ}.

Analysis:
Using Thevenin,

$$V_{GG} = \frac{R_2}{R_1 + R_2} V_{DD} = 6 \text{ V}$$

We can write the equations

$$V_{GG} = v_{GSQ} + R_S i_{DQ} = 6,$$

$$V_{DD} = (R_D + R_S) i_{DQ} + v_{DSQ} = 2R_D i_{DQ} + v_{DSQ} = 12$$

Assuming saturation conditions, the current i_D can be written as

$$i_{DQ} = K(v_{GSQ} - V_T)^2 \Rightarrow v_{GSQ} + R_S K(v_{GSQ} - V_T)^2 = 6 \Rightarrow 10v_{GSQ}^2 - 19v_{GSQ} + 4 = 0 \Rightarrow$$

$$v_{GSQ} = 1.66 \text{ V}$$

The other solution is not acceptable because less then V_T.

It follows

$$i_{DQ} = \frac{6 - v_{GSQ}}{R_S} = 0.434 \text{ mA},$$

$$v_{DSQ} = 12 - 2R_D i_{DQ} = 3.32 \text{ V}$$

Section 11.4: MOSFET Switches

Problem 11.15

Solution:

Known quantities:
The CMOS NAND gate of Figure 11.21.

Find:
Identify the state of each transistor for $v_1 = v_2 = 5$ V.

Analysis:
The two transistors at the top are cut off and the two at the bottom are on.

Problem 11.16

Solution:

Known quantities:
The CMOS NAND gate of Figure 11.21.

Find:
Identify the state of each transistor for v_1=5V, v_2=0V.

Analysis:
The transistor at the bottom and the first on the top are off, the other two are on.

Problem 11.17

Solution:

Find:
Draw the schematic diagram of a two-input CMOS OR gate.

Analysis:
The output of the circuit of Figure 11.18 is connected as an input to the circuit of Figure 11.14.

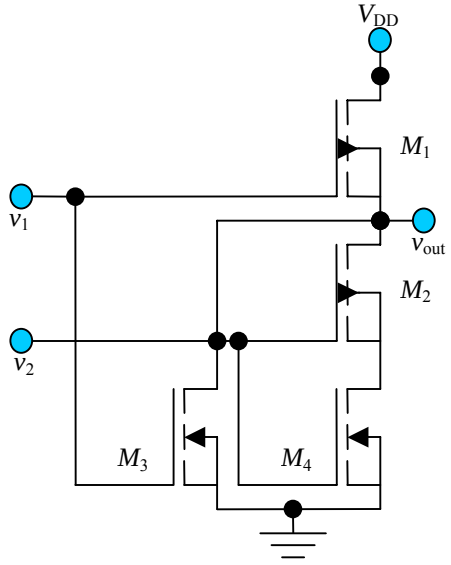


Figure 11.18

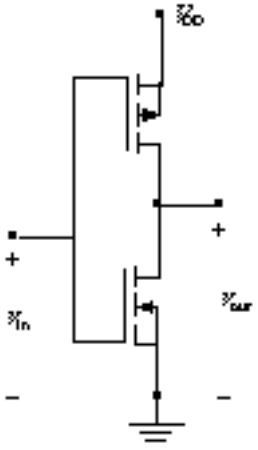


Figure 11.14

Problem 11.18

Solution:

Find:
Draw the schematic diagram of a two-input CMOS AND gate.

Analysis:
The output of the circuit of Figure 11.21 is connected as an input to the circuit of Figure 11.14.

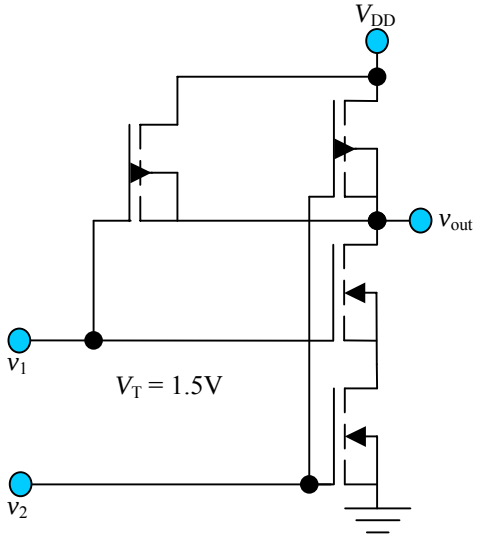


Figure 11.21

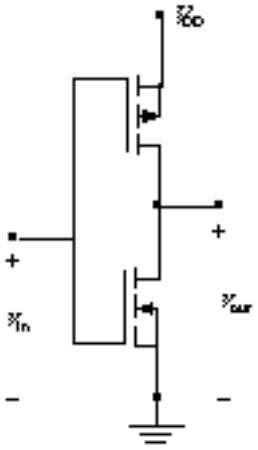


Figure 11.14

Problem 11.19

Solution:

Find:
Draw the schematic diagram of a two-input CMOS NOR gate.

Analysis:
The circuit of Figure 11.18

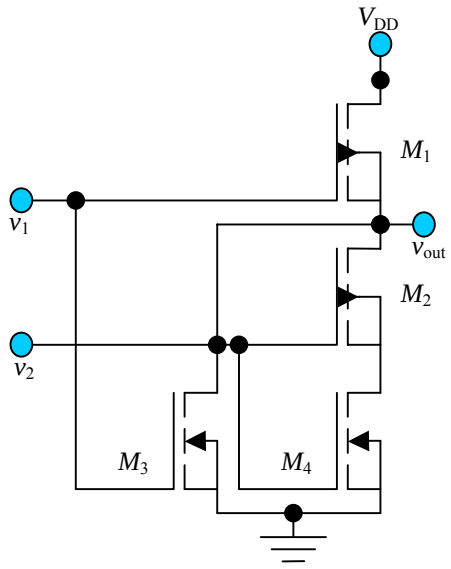


Figure 11.18

Problem 11.20

Solution:

Find:
Draw the schematic diagram of a two-input CMOS NAND gate.

Analysis:
The circuit of Figure 11.21.

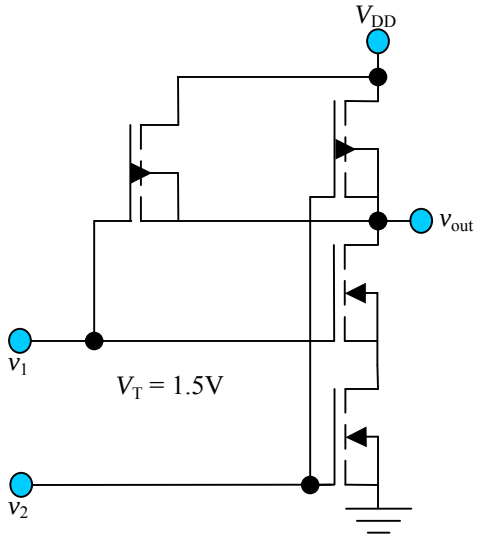


Figure 11.21

Problem 11.21

Solution:

Known quantities:
The circuit of Figure P11.21.

Find:
Show that the given circuit functions as a logic inverter.

Analysis:
Construct a state table:

v_{in}	Q_1	Q_2	v_{out}
low	resistive	open	high
high	open	resistive	low

This table clearly describes an inverter.

Problem 11.22

Solution:

Known quantities:
The circuit of Figure P11.22.

Find:
Show that the given circuit functions as a NOR gate.

Analysis:
Construct a state table:

v_1	v_2	Q_1	Q_2	v_{out}
0	0	off	off	high
0	high	off	on	low
high	0	on	off	low
high	high	on	on	low

This table clearly describes a NOR gate.

Problem 11.23

Solution:

Known quantities:
The circuit of Figure P11.23.

Find:
Show that the given circuit functions as a NAND gate.

Analysis:
Construct a state table:

v_1	v_2	Q_1	Q_2	v_{out}
0	0	off	off	high
0	high	off	on	high

high	0	on	off	high
high	high	on	on	low

This table clearly describes a NAND gate.
